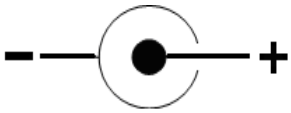
PA5750 EVB

Evaluation Board User Manual

Rev. 2.0

IMPORTANT:

A DC POWER Adaptor must be used when evaluating PA5750 EVB. The voltage of this DC power must be +5V, and the current must be 500mA or higher. The diagram of DC power jack plug is showed as below.



Exceeding +5v Voltage can damage the EVB components. Lower voltage will cause improper operation of some or all EVB components.

Date	Document	Version	Author

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USER MANUAL OF PA5750 EVB

INTRODUCTION

PA5750 is a stereo CODEC for portable audio application.

The EVB has been designed to allow the user ease of use and give optimum performance in device measurement as well as providing the user with the ability to listen to the excellent audio quality offered by the PA5750.

GETTING STARTED

EVALUATION BOARD CHECKLIST

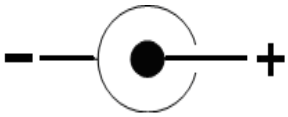
The following items are available from ProTek Analog.

- PA5750 EVB
- PA5750 Control Software version 1.0 or PA5750 Control Software version 2.0
- PA5750 User Manual

CUSTOMER REQUIREMENTS

- DC Power Supply of +5V
- PC with RS-232 Port and RS-232(9 PIN) cable
- Digital Coaxial source like DVD player with S/P DIF out
- Analog Coaxial Source or 3.5mm Jack plug signal source like microphone
- Stereo Headphone with 3.5mm jack plug
- Digital coaxial data receive unit like AP2722 instrument

Power Supply

JACK	Description
J700	+5v/500mA DC Power 

Board Inputs

JACK	Description
J400	S/PDIF IN(digital signal)
J500	LIN1/RIN1(Analog signal)
J501	
J503	LIN2RIN2(Analog signal)
J504	
J506	LIN3/RIN3(Analog signal)
J507	
J502	Microphone Input
J505	Microphone Input
J508	Microphone Input

Board Outputs

JACK	Description
J401	S/PDIF Out(digital signal)
L1OUT	LOUT1/ROUT1(Analog signal)
R1OUT	
L2OUT	LOUT2/ROUT2(Analog signal)
R2OUT	
MONO	MONO OUT/OUT3(Analog signal)
OUT3	
	HEADPHONE OUT
	HEADPHONE OUT
	HEADPHONE OUT

SWITCH

SWITCH	PIN	Description
SW200	1	Set PA5750 to Slave or Master Mode, Refer to the explanation on EVB.
	2	Set DAC's MCLK/LRCK ratio, Refer to the explanation on EVB.
	3	Set DAC to I2S-24bit/Left Justified-24bit/Right Justified-24bit , Refer to the explanation on EVB.
	4	
SW201	1	SET ADC's MCLK/LRCK ratio, Refer to the explanation on EVB.
	2	
	3	Set ADC to I2S-24bit/Left Justified-24bit/Right Justified-24bit , Refer to the explanation on EVB.
	4	

Important: SW200 and SW201 are settled before power up.

CLOCK HEADER

JP300

GND	1	2
SCLK	3	4
GND	5	6
DLRCK	7	8
GND	9	10
MCLK	11	12
GND	13	14
DSDIN	15	16

JP301

GND	1	2
ASDOUT	3	4
GND	5	6
ALRCK	7	8

HEADER	PIN	Description
JP300	SCLK	Pin3 Shorted with Pin4 when Master or Slave mode
	DLRCK	Pin7 Shorted with Pin8 when Master or Slave mode
	MCLK	Pin11 Shorted with Pin12 when Master or Slave mode
	DSDIN	Pin15 Shorted with Pin16 when Master or Slave mode
JP301	ALRCK	Pin1 Shorted with Pin2 when Slave mode
	ASDOUT	Pin5 Shorted with Pin6 when Master or Slave mode

Important:

If you need to connect the external clock to PA5750 EVB, you should remove the short circuit line on the JP300 and JP301 first, then connect the external clock to pin4, pin8, pin12, pin16 of JP300 and pin2, pin6 of JP301.

JP300 and JP301 are set before power up.

ADC&DAC Data HEADER

JP302

DSDIN	1	2
ASDOUT	3	4

HEADER	PIN	Description
JP302	DSDIN	The Data In of DAC, Pin1 shorted to Pin2 when DAC is used.
	ASDOUT	The Data out of ADC, Pin3 shorted with Pin4 when ADC is used.

Important:

If you need to set the ADC and DAC in “ADC to DAC loop back” mode, you should short pin2 and pin4 of JP302.

JP302 is set before power up.

Headphone plug-in detection Jumper

JP607&JP613

1	**2**
3	**4**

JP606

1	**2**
3	**4**
5	**6**

JUMPER	PIN	Description
JP606	3	Pin3 Shorted with Pin4, Headphone be connected to LOUT2/ROUT2 of PA5750
	4	
	5	Pin5 Shorted with Pin6,Headphone be connected to LOUT1/ROUT1 of PA5750
	6	
JP607&JP613	1	Pin1 Shorted with Pin2 ,High Level for Headphone detection
	2	
	3	Pin3 Shorted with Pin4 ,Low Level for Headphone detection
	4	

Other Jumpers

There are some jumpers on PA5750 EVB. Please refer to the “Jumper setting for PA5750EVB” document.

KEYPAD

A MCU (STC89LE51RC+) is mounted PA5750 EVB. This MCU can communicate with PC via RS232 cable and can read or write to PA5750 via I2C or SPI bus.

9 KEYPAD (push-buttons) are assembled in PA5750 EVB. The function of this KEYPAD is listed below.

KEYPAD	FUNCTION
K200	RESET MCU
K201	CODEC
K202	VOLUME DOWN
K203	ADC (The Input of ADC is LIN2/RIN2)
K204	VOLUME UP
K205	DAC
K206	DAC MUTE
K207	BYPASS(DAC bypass, LINE IN or Microphone In to Line Out or Headphone
K208	Power Down

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SET Communication Mode between MCU and PA5750

PA5750 can communicate with the host MCU via the control port of PA5750.This control port can be used as I2C or SPI bus.

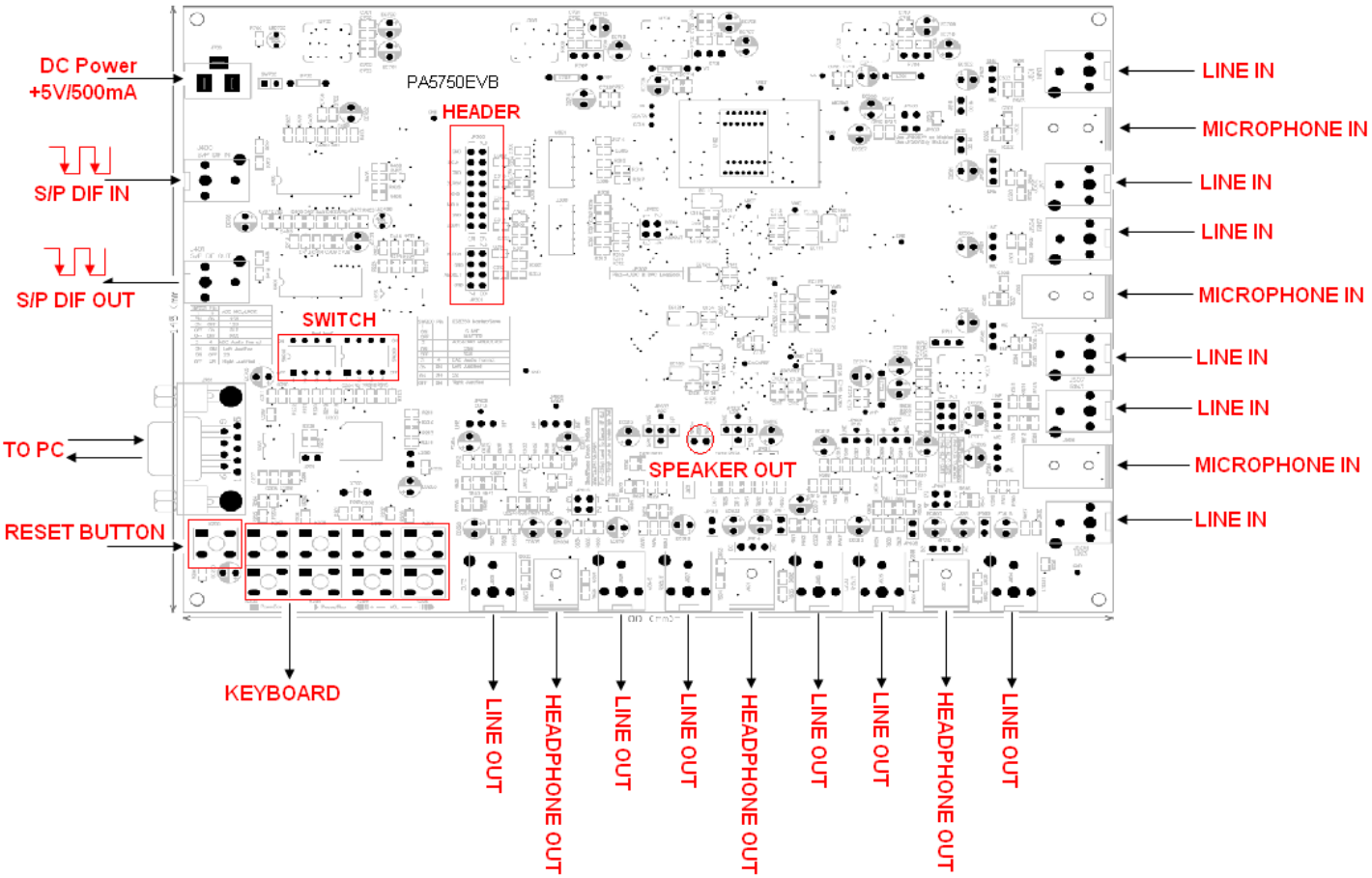
J201 of PA5750 EVB is used to set the communication mode to I2C or SPI.

HEADER	STATE	Description
J201	OPEN	SPI
	SHORT	I2C

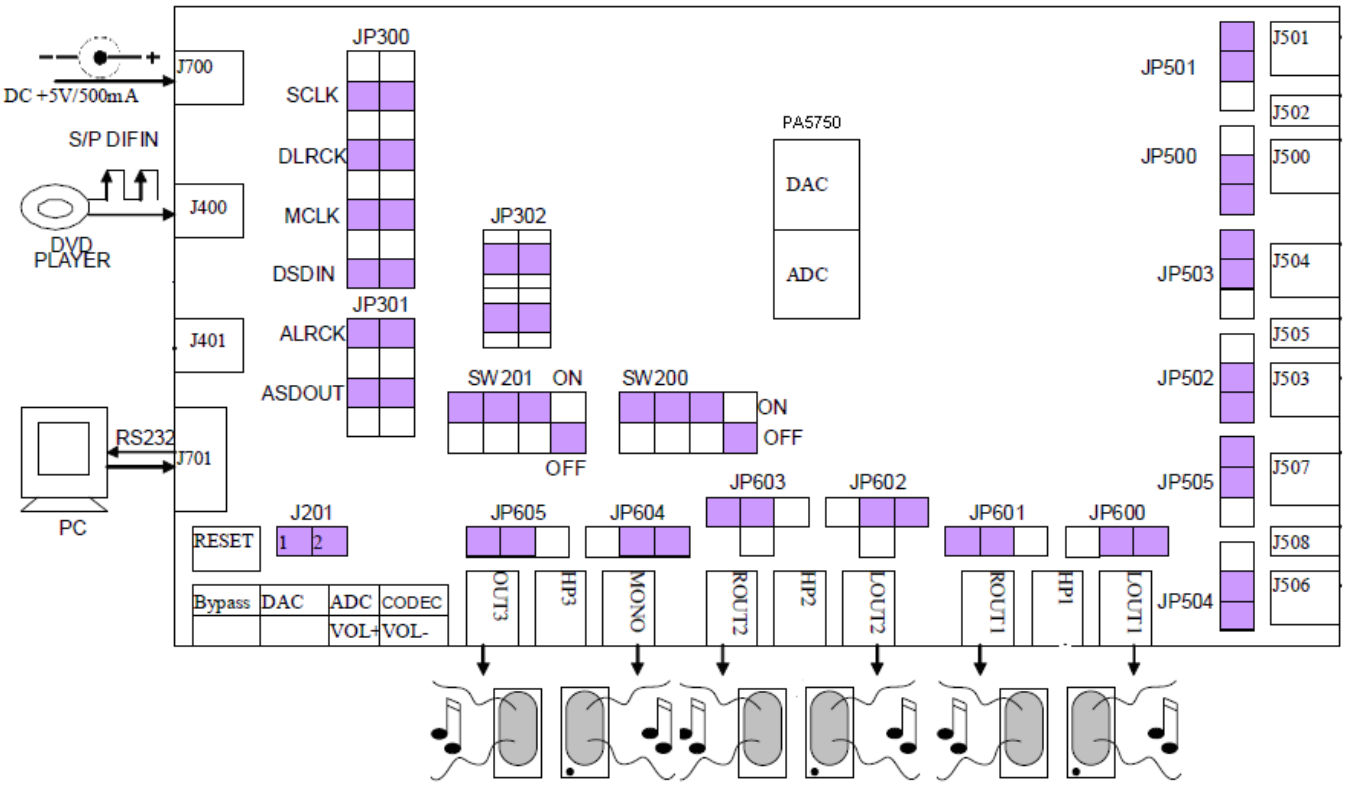
Important:

If SPI mode is selected, the host mcu can write to PA5750 via SPI only. If I2C mode is selected, the host mcu can write or read PA5750 via I2C.

INTERFACE PA5750 EVB Layout



DAC SETUP (SLAVE MODE, I2S-24BIT, MCLK/LRCK=256, DAC to LINE OUT)



Important:

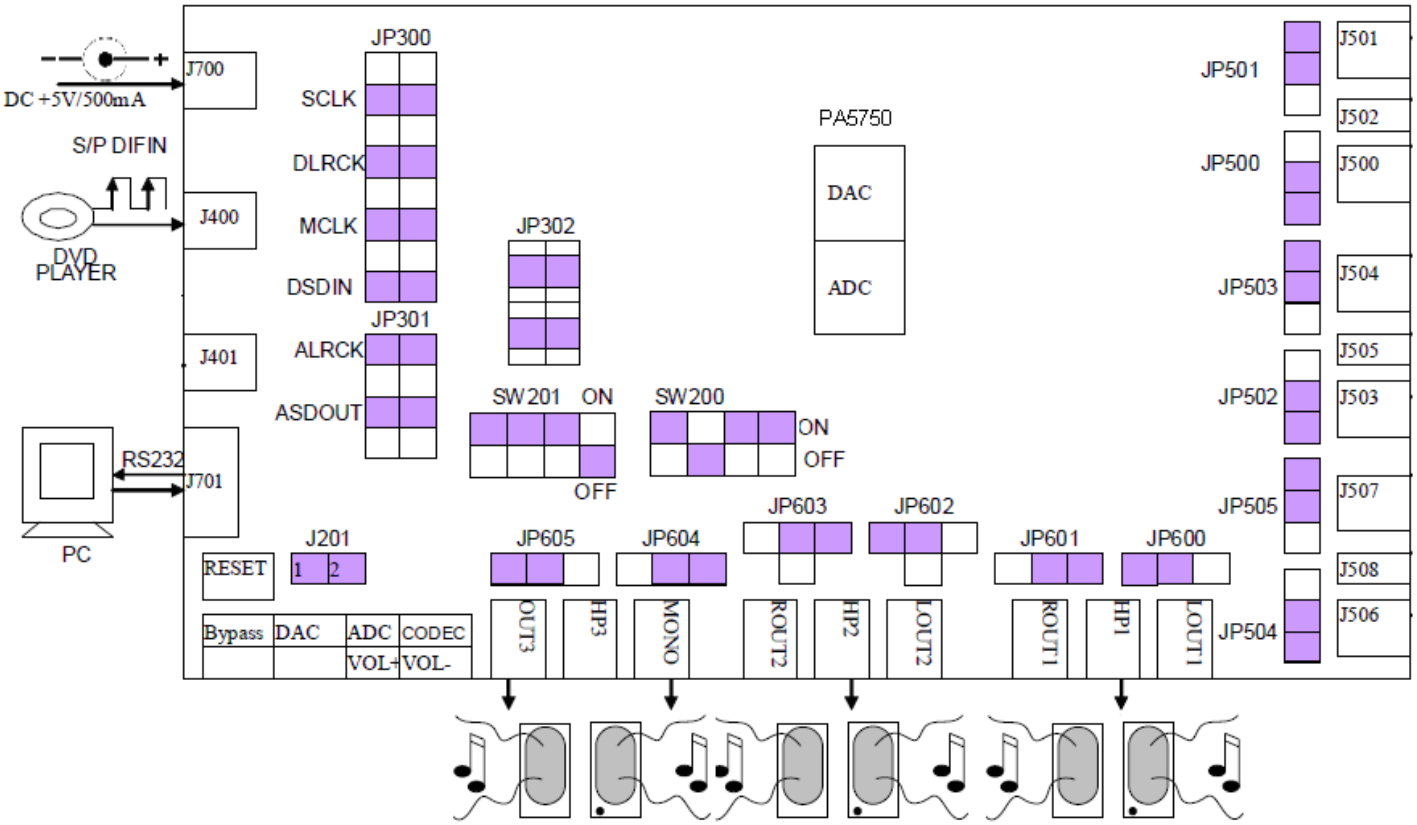
The S/PDIF IN of J400 must be required to provide clock and data for the PA5750 digital audio interface.

If you should set the headphone AC or DC coupled Jumper, please refer to "Jumper setting for PA5750EVB".

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

DAC SETUP (SLAVE MODE, Left Justified-24BIT, MCLK/LRCK=128, LOUT1&ROUT1&LOUT2&ROUT2 to Headphone)



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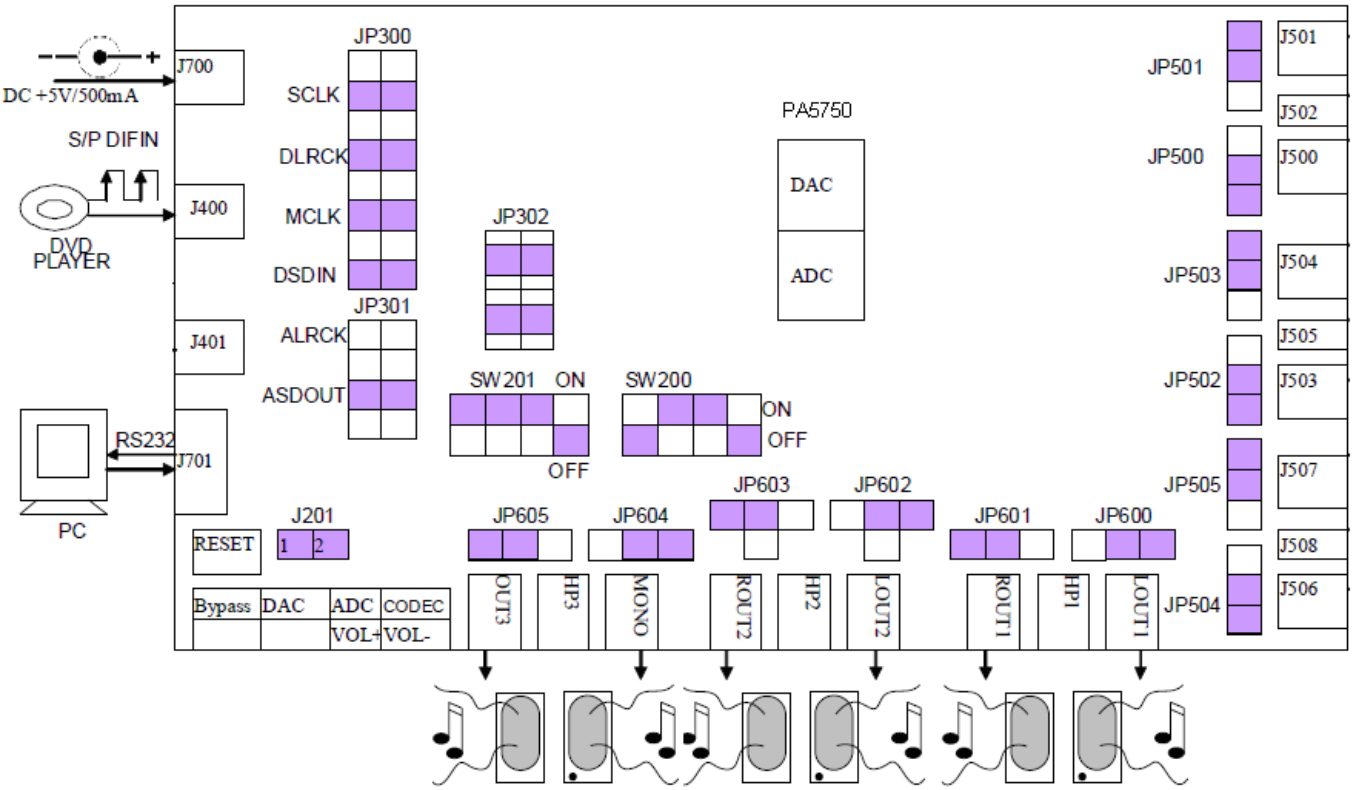
If you should set the headphone AC or DC coupled Jumper, please refer to "Jumper setting for PA5750EVB".

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

DAC SETUP (MASTER MODE, I2S-24BIT, MCLK/LRCK=256, DAC to LINE OUT)



Important:

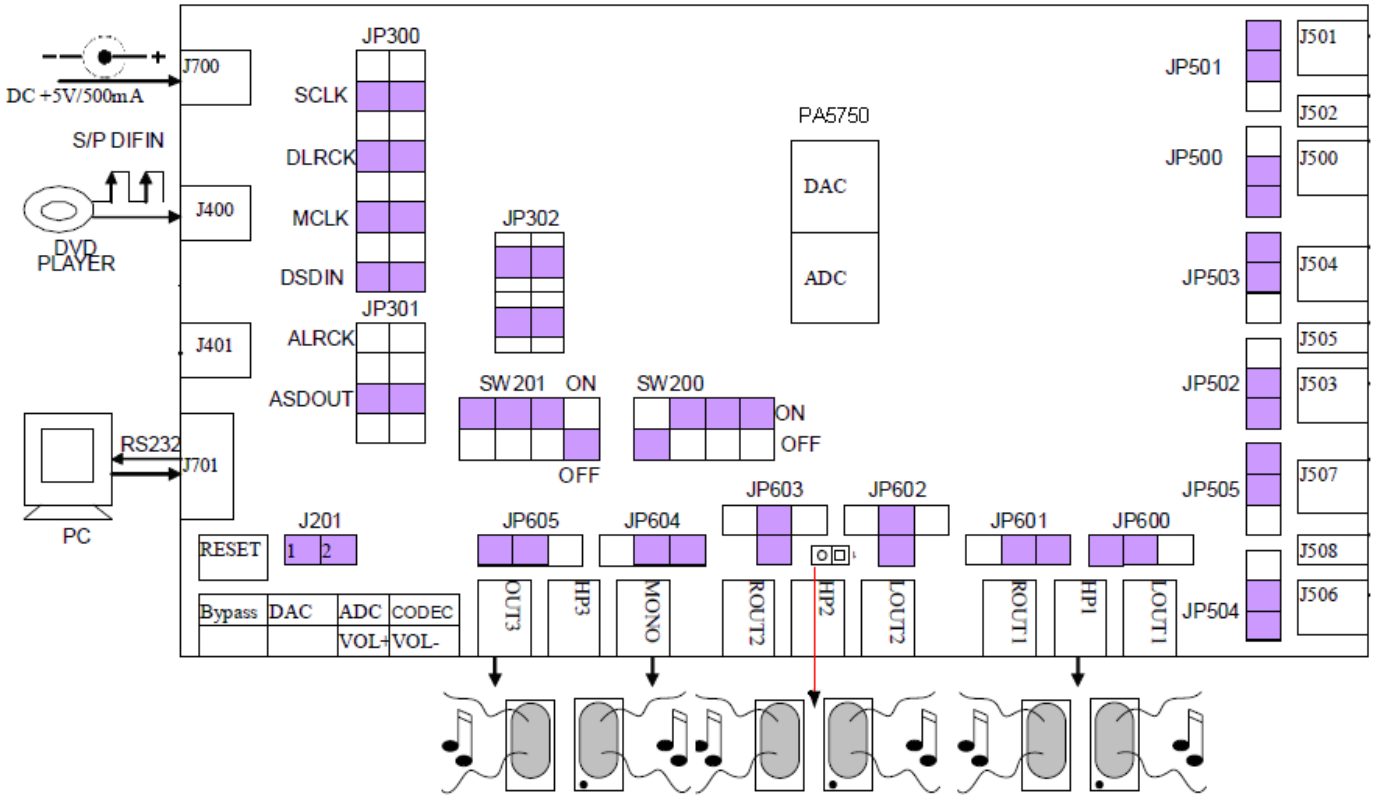
The S/PDIF IN of J400 is required to provide clock and data for the PA5750 digital audio interface.

If you should set the headphone AC or DC coupled Jumper, please refer to "Jumper setting for PA5750EVB".

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

DAC SETUP (MASTER MODE, Left Justified -24BIT, MCLK/LRCK=256, LOUT1&ROUT1 to Headphone, LOUT2&ROUT2 to Speaker)



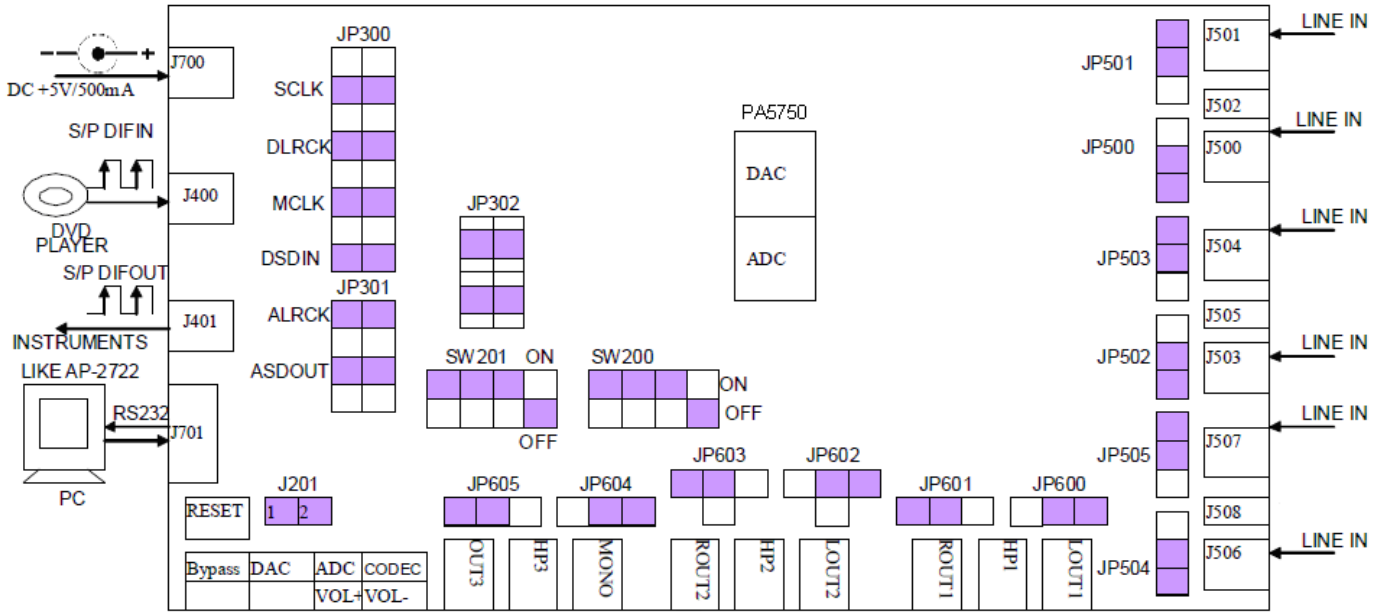
Important:

The S/PDIF IN of J400 must be required to provide clock and data for the PA5750 digital audio interface.

If you should set the headphone AC or DC coupled Jumper, please refer to "Jumper setting for PA5750EVB".

This setting must be done before power up.

ADC SETUP(SLAVE MODE,I2S-24BIT,MCLK/LRCK=256,LINE IN to ADC)



Important:

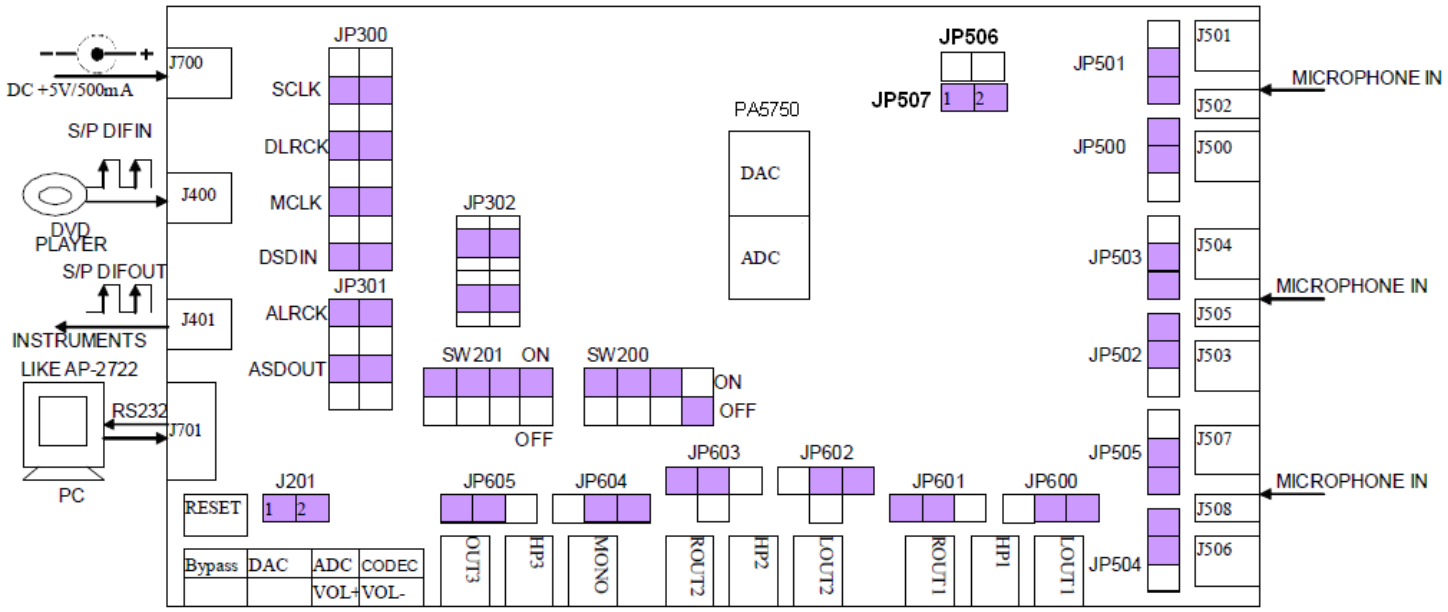
The S/PDIF IN of J400 is required to provide clock for the PA5750 digital audio interface.

Refer to "Jumper setting for PA5750EVB" document to set microphone in or line in jumper.

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

ADC SETUP (SLAVE MODE, Left Justified-24BIT, MCLK/LRCK=256, Microphone IN to ADC)



Important:

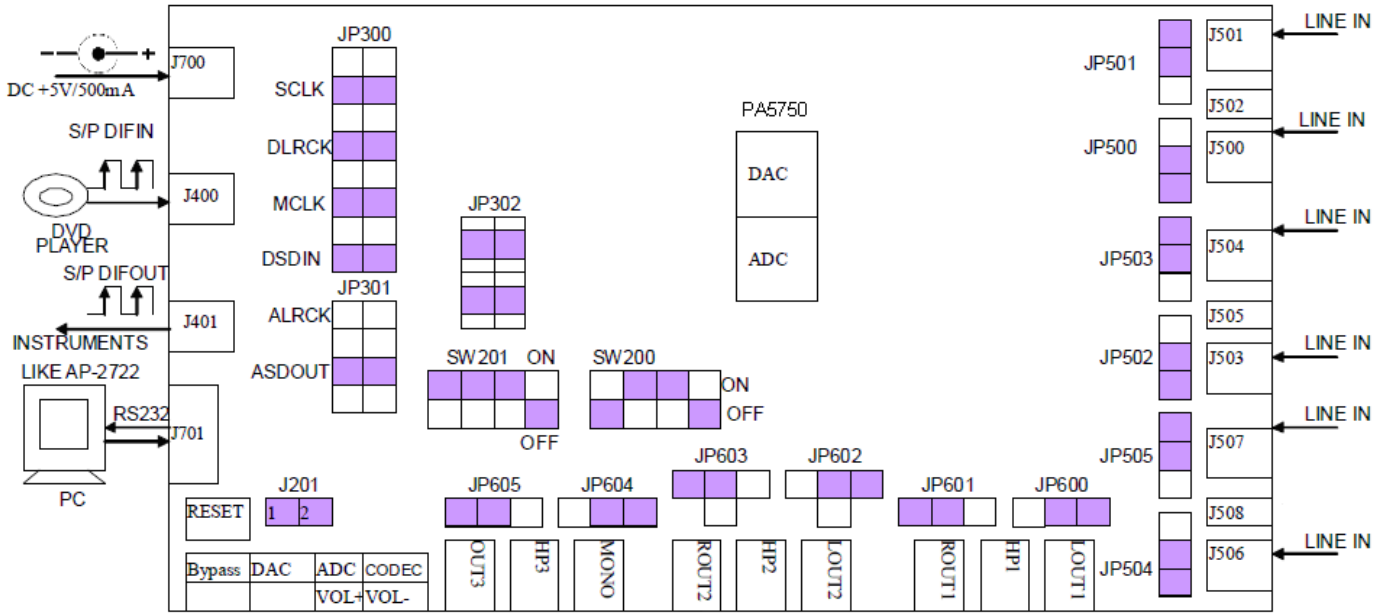
The S/PDIF IN of J400 is required to provide clock for the PA5750 digital audio interface.

Refer to "Jumper setting for PA5750EVB" document to set microphone in or line in jumper.

If using the Mic-Bias output of PA5750, please short JP507. If using VA as Mic-Bias, please short JP506 and remove the short circuit line on JP507.

This setting must be done before power up.

ADC SETUP (MASTER MODE, I2S-24BIT, MCLK/LRCK=256, LINE IN to ADC)



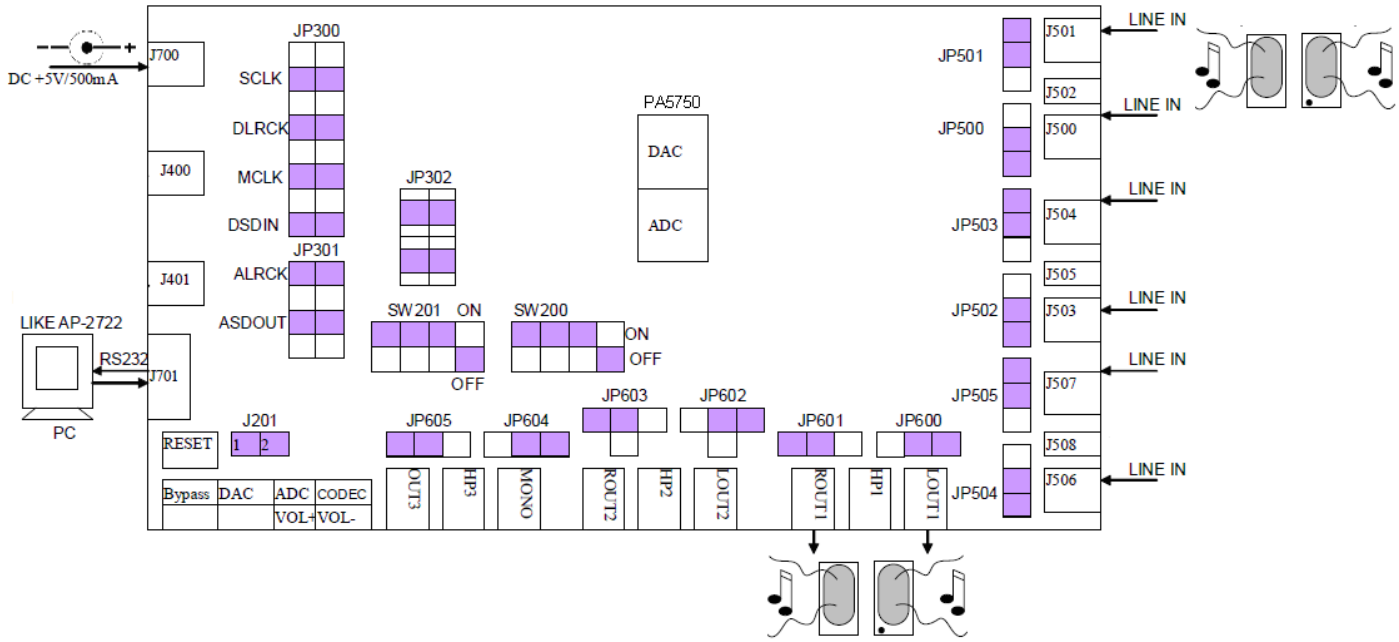
Important:

The S/PDIF IN of J400 is required to provide clock for the PA5750 digital audio interface.

Refer to "Jumper setting for PA5750EVB" document to set microphone in or line in jumper.

This setting must be done before power up.

BYPASS SETUP (LINE IN or Microphone IN to LINE OUT, Bypass DAC)



Important:

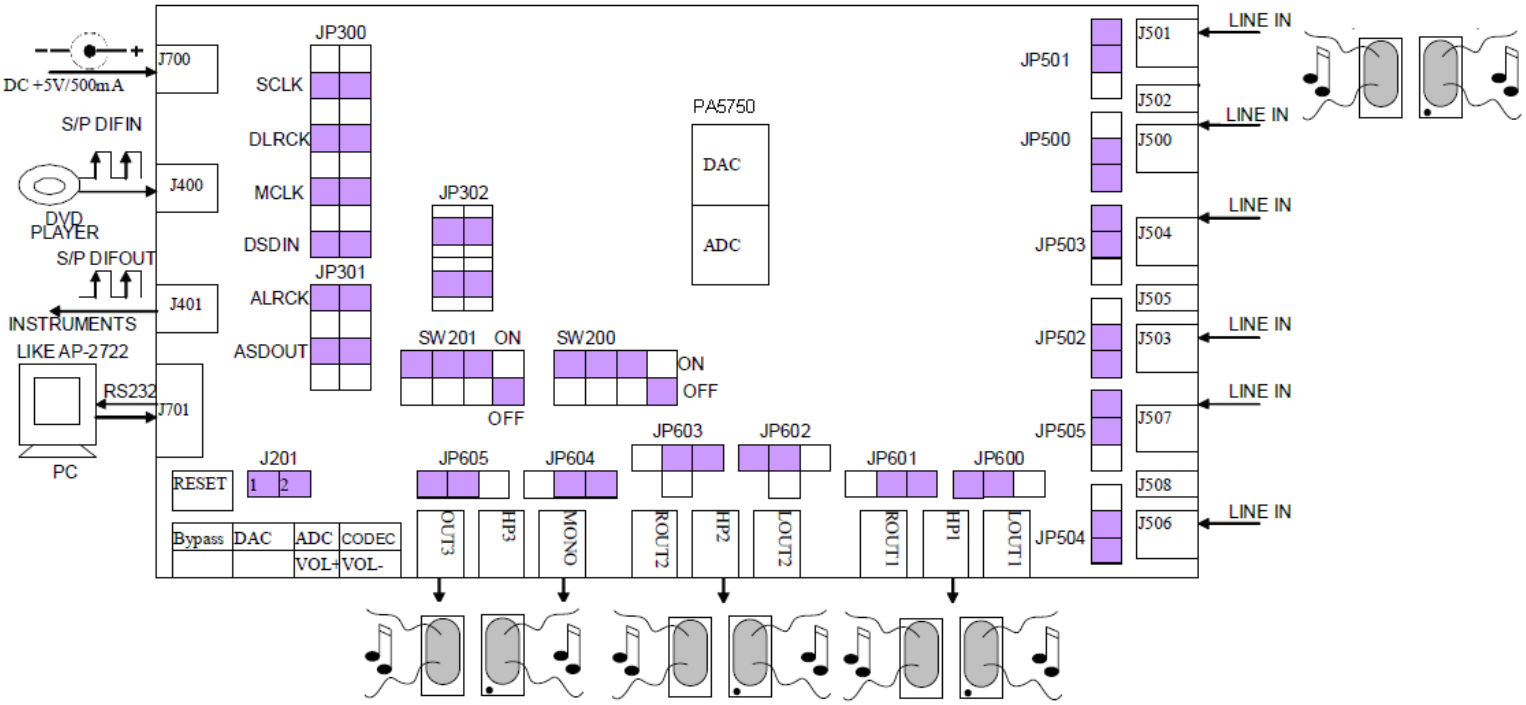
In Bypass Mode, the DAC will be bypassed. The Line In or Microphone In signals are routed to Line out or headphone out.

If you should set the headphone AC /DC coupled Jumper or Microphone/LINE IN jumper, please refer to "Jumper setting for PA5750EVB".

This setting must be done before power up

USER MANUAL OF PA5750 EVB

CODEC SETUP (SLAVE MODE, DAC&ADC in I2S-24BIT, MCLK/LRCK=256 Mode, LINE IN to ADC, DAC to Headphone)



Important

The S/PDIF IN of J400 is required to provide clock and data for the PA5750 digital audio interface.

If you want to change DAC or ADC to Left-justified or Right-Justified Format, please refer to DAC SETUP or ADC SETUP chapter.

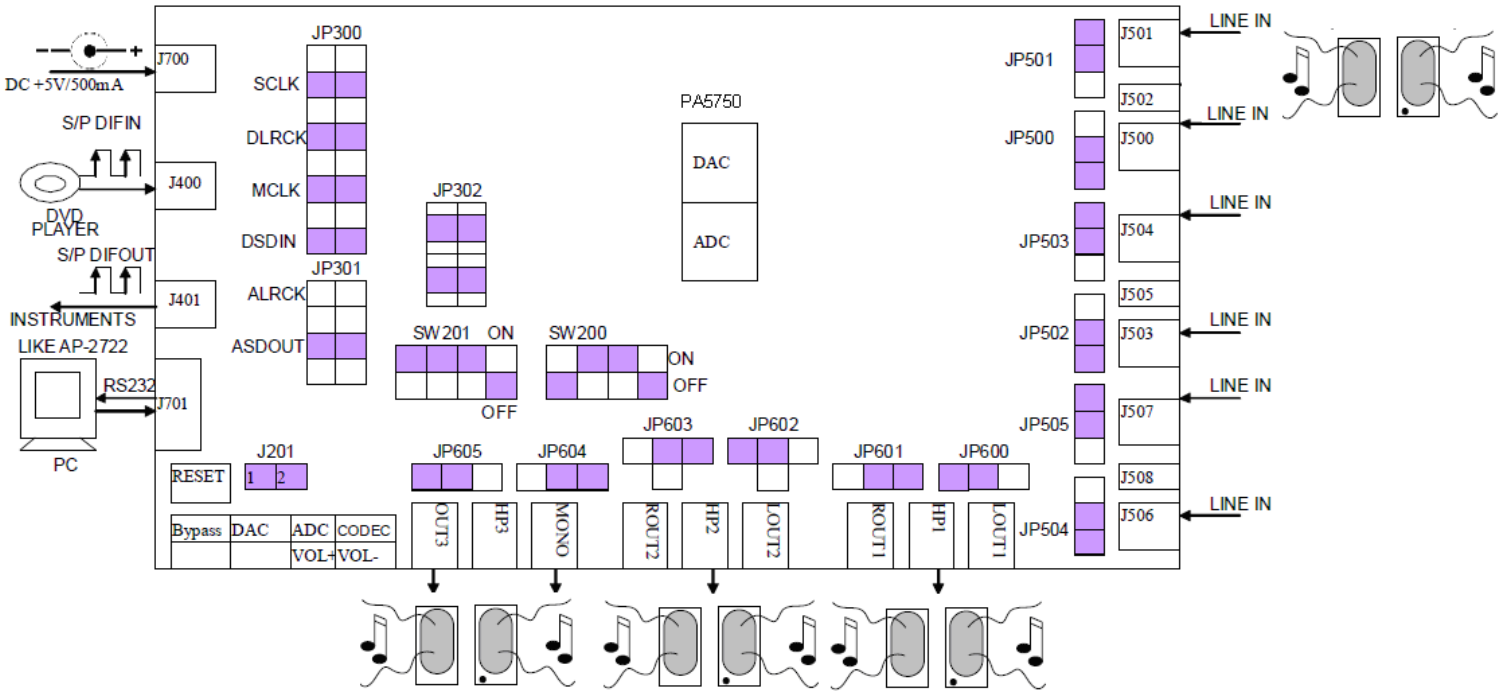
If you want to change DAC or ADC's MCLK/LRCK ratio, please refer to DAC SETUP or ADC SETUP chapter also.

If ADC or DAC's Mode has been changed, please power up the PA5750 EVB again.

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

CODEC SETUP (MASTER MODE, DAC&ADC in I2S-24BIT, MCLK/LRCK=256 Mode, LINE IN to ADC, DAC to Headphone)



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If you want to change DAC or ADC to Left-justified or Right-Justified Format, please refer to DAC SETUP or ADC SETUP chapter.

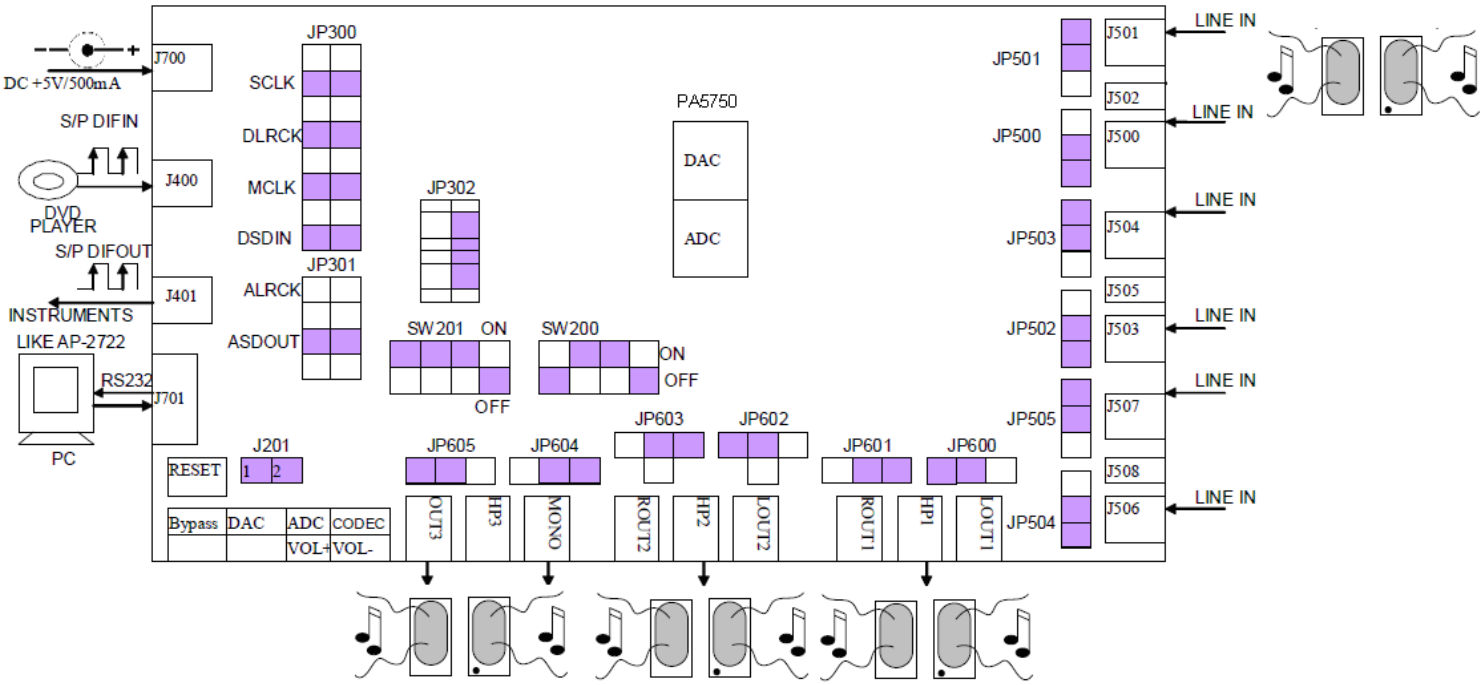
If you want to change DAC or ADC's MCLK/LRCK ratio, please refer to DAC SETUP or ADC SETUP chapter also.

If ADC or DAC's Mode has been changed, please power up the PA5750 EVB again.

This setting must be done before power up.

USER MANUAL OF PA5750 EVB

CODEC SETUP (MASTER MODE, DAC&ADC in I2S-24BIT, MCLK/LRCK=256 Mode, ADC and DAC LoopBack, LINE IN to ADC, DAC to Headphone)



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If you want to change DAC or ADC's MCLK/LRCK ratio, please refer to DAC SETUP or ADC SETUP chapter also.

If ADC or DAC's Mode has been changed, please power up the PA5750 EVB again.

This setting must be done before power up.

TEXT Console

A TXT file can be used to configure PA5750.The format of text file is showed as below.

- **Write Register**

:wRRDD@

Notes:

The “w” is lowercase. The “RR” is the Hex address of Register. The “DD” is the Hex data of Register data.

- **RESET CLOCK Generator**

:D0E00@

Notes:

The “D” is uppercase

- **UN-RESET CLOCK Generator**

:D0F00@

Notes:

The “D” is uppercase

The RESET command and UN-RESET command must be used in pairs.

- **Console text example**

PA5750 can be configured as CODEC if the text file listed below is used.

:D0E00@ ⟶ be used in pairs with :D0F00@
:w0800@
:w0005@
:w0140@
:w02FF@
:w0300@
:w043F@
:w0900@
:w0A00@
:w0B02@
:w0C00@

```
:w0D02@
:w1000@
:w1100@
:w1700@
:w1802@
:w1A00@
:w1B00@
:w2600@
:w27B8@
:w2838@
:w2938@
:w2A38@
:w2B38@
:w2CB8@
:w2D90@
:w2E1E@
:w2F1E@
:w301E@
:w311E@
:w321E@
:w0200@
:D0F00@
```

- **“OPEN File” button**

  Click “OPEN FILE” button, the text file should load into buffer of Evaluation software.
- **“SEND” button**

  Click “SEND” button, the content of the text file will be sent to PA5750EVB if PA5750EVB is connected to PC via RS-232 cable. Then the MCU assembled on PA5750EVB will write the register of PA5750 or reset/un-reset clock generator.