

### Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.6Ω.
- V<sub>CC</sub> Range: 1.8V to 4.2V
- Rail-to-Rail Signal Range
- High Off Isolation: -75dB @ 100kHz
- Crosstalk Rejection: -90dB @ 100kHz
- Break-Before-Make Switching
- Extended Industrial Temperature Range: -40°C to 85°C
- LoPro® Packaging (Pb-free): 10-Lead Micro Package
- QFN-10Lead Micro Package

### Applications

- Cell Phones
- PDAs
- MP3 players
- Portable Instrumentation
- Computer Peripherals
- Speaker Headset Switching
- Power Routing
- Relay Replacement
- Audio and Video Signal Routing
- PCMCIA Cards
- Modems

### Pin Descriptions

Pin No.	Name	Description
1,3	NO <sub>x</sub>	DATA Port (Normally Open)
4	GND	Ground
10,2	NC <sub>x</sub>	DATA Port (Normally Closed)
8,5	COM <sub>x</sub>	Common Port / DATA Port
9	V <sub>CC</sub>	Positive Power Supply
7,6	IN <sub>x</sub>	Logic Control

### Logic Function Table

Logic Input (IN <sub>x</sub> )	Function
0	NC <sub>x</sub> Connected to COM <sub>x</sub>
1	NO <sub>x</sub> Connected to COM <sub>x</sub>

### Description

ProTek Analog's PAM22LOPR2268 is a dual high-bandwidth, fast single-pole double throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch.

Specified over a operating power supply voltage, 1.8V to 4.2V, the PAM22LOPR2268 has an On-Resistance of 0.6Ω at +2.7V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

### Functional Block Diagram

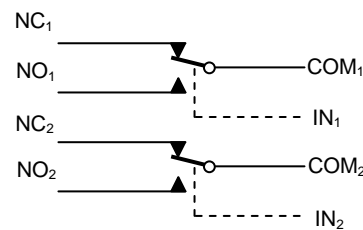
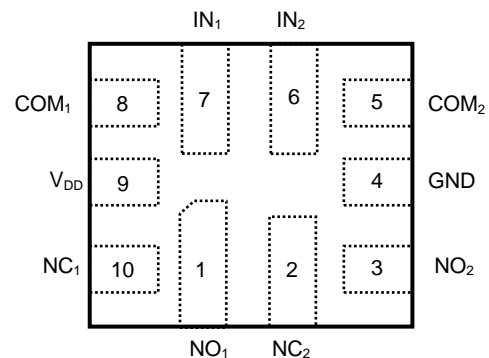


Fig. 1 PAM22LOPR2268

### Pin Configuration (Top View)



### Ordering Information

Temp Range	Package	Part Number
-40 to 85 °C	QFN-10	PAM22LOPR2268Q-T7
-40 to 85 °C	10 Lead LoPro	PAM22LOPR2268-T7

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage $V_{CC}$	4.5V
DC Switch Voltage (VS) <sup>(2)</sup>	$V_{CC} + 0.5V$
DC Input Voltage (VIN) <sup>(2)</sup>	4.5V
Analog Signal Range	Min -1.0 to Max $V_{CC} + 1.0$
Continuous Current NO_NC_COM_	$\pm 300mA$ Peak
Current NO_NC_COM_ (pulsed at 1ms 50% duty cycle)	$\pm 400mA$ Peak
Current NO_NC_COM_ (pulsed at 1ms 10% duty cycle)	$\pm 500mA$
Storage Temperature Range (TSTG)	-65°C to +150°C
Junction Temperature under Bias (TJ)	150°C
Junction Lead Temperature (TL) (Soldering, 10 seconds)	260°C
Power Dissipation (PD) @ +85°C	250mW

**Recommended Operating Conditions<sup>(3)</sup>**

Supply Voltage Operating ( $V_{CC}$ )	1.8V to 4.2V
Control Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$ Switch Input Voltage ( $V_{IN}$ )
Output Voltage ( $V_{OUT}$ )	-0.3V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
Control Input $V_{CC} = 2.3V - 3.6V$	0ns/V to 10ns/V
Thermal Resistance ( $\theta_{JA}$ )	350°C/W
Lead Temperature (soldering 10s)	+240°C
Bump Temperature (soldering notes)	
Infrared (15s)	+220°C
Vapor Phase (60ns)	+215°C

**Notes:**

- "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
- Control input must be held HIGH or LOW; it must not float.
- Internal Resistance  $R_{TERM}$  is guaranteed by design and not production tested.

**Capacitance**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NC Off Capacitance	$C_{NC(OFF)}$	$f = 1MHz$ , See Test Circuit Figure7.		35		pF
NO Off Capacitance	$C_{NO(OFF)}$	$f = 1MHz$ , See Test Circuit Figure7.		35		
NC On Capacitance	$C_{NC(ON)}$	$f = 1MHz$ , See Test Circuit Figure8.		95		
NO On Capacitance	$C_{NO(ON)}$	$f = 1MHz$ , See Test Circuit Figure8.		95		

**DC Electrical Characteristics +3V Supply**
*(V<sub>CC</sub> = 2.7V to 3.3V, T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at 3V and +25°C.)*

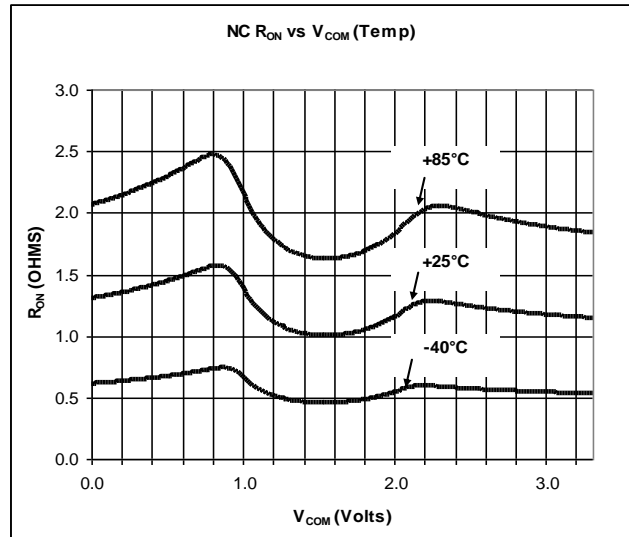
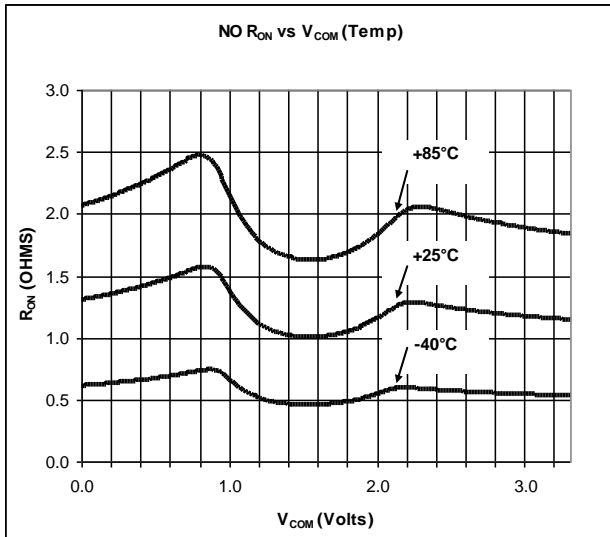
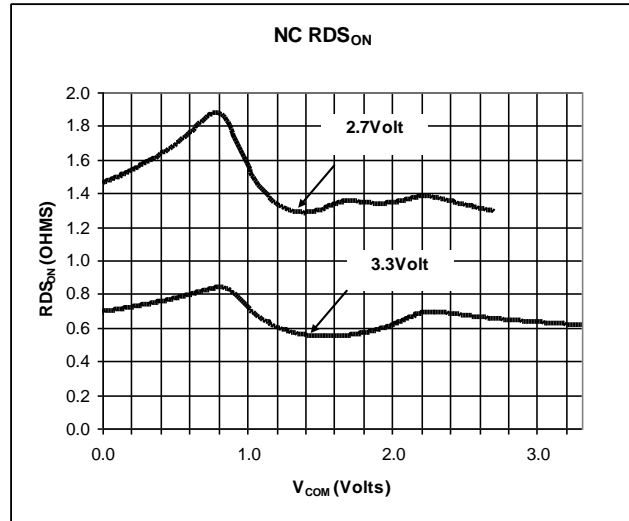
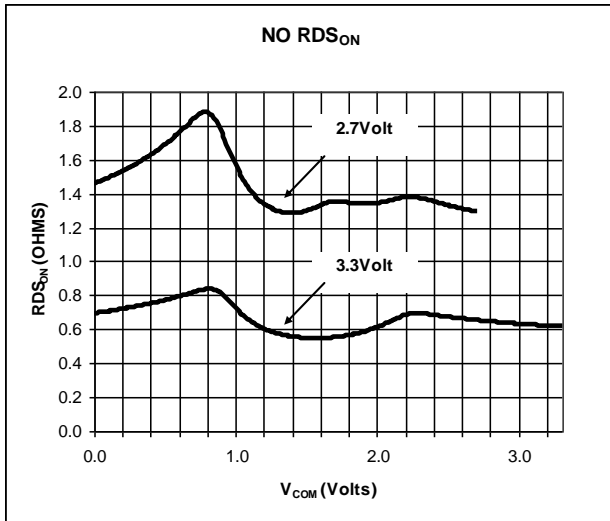
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Analog Switch</b>						
Analog Signal Range	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		-0.3		V <sub>CC</sub>	V
NC On-Resistance	R <sub>ON(NC)</sub>	V <sub>CC</sub> = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NC</sub> = 0 to V <sub>CC</sub>		0.4	0.6	Ω
NO On-Resistance	R <sub>ON(NO)</sub>	V <sub>CC</sub> = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> = 0 to V <sub>CC</sub>		0.4	0.6	
On-Resistance Match Between Channels	ΔR <sub>ON</sub>	V <sub>CC</sub> = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V		0.01	0.05	
NC On-Resistance Flatness	R <sub>ONF(NC)</sub>	V <sub>CC</sub> = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NC</sub> = 0 to V <sub>CC</sub>			0.2	
NO On-Resistance Flatness	R <sub>ONF(NO)</sub>	V <sub>CC</sub> = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> = 0 to V <sub>CC</sub>			0.2	
Internal Termination Resistors	R <sub>TERM</sub>			200		
NO or NC Off Leakage Current	I <sub>OFF(NO)</sub> or I <sub>OFF(NC)</sub>	V <sub>CC</sub> = 3.3V, I <sub>COM</sub> , V <sub>NO</sub> or V <sub>NC</sub> = 3.0V, 0.3V V <sub>COM</sub> = 0.3V, 3.0V	-20		20	nA
COM On Leakage Current	I <sub>COM(ON)</sub>	V <sub>CC</sub> = 3.3V, I <sub>COM</sub> , V <sub>NO</sub> or V <sub>NC</sub> = 3.0V, 0.3V V <sub>COM</sub> = 0.3V, 3.0V or Floating	-20		20	
<b>Digital I/O</b>						
Input Logic High	V <sub>IH</sub>		1.3			V
Input Logic Low	V <sub>IL</sub>				0.5	
Input Hysteresis	V <sub>H</sub>	V <sub>CC</sub> = 3.3V		300		mV
IN Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 or V <sub>CC</sub>	-0.5		0.5	μA
Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0 or V <sub>CC</sub>		0.9	1.2	nA

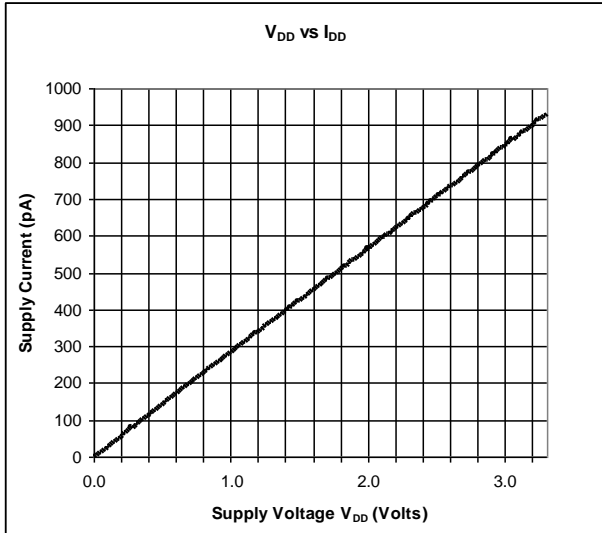
**Switch and AC Characteristics**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Time	t <sub>ON</sub>	V <sub>CC</sub> = 2.7V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF. See Test Circuit Figure 1 & 2		15	25	nS
Turn-Off Time	t <sub>OFF</sub>	V <sub>CC</sub> = 2.7V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF. See Test Circuit Figure 1 & 2		4	10	
Break-Before-Make Delay	t <sub>BBM</sub>	V <sub>CC</sub> = 2.7V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF. See Test Circuit Figure 3			20	
Charge Injection	Q	COM = 0, R <sub>S</sub> = 0, C <sub>L</sub> = 1nF. V <sub>GEN</sub> = 0 See Test Circuit Figure 4		55		pC
Off-Isolation	Q <sub>IRR</sub>	C <sub>L</sub> = 5pF, R <sub>L</sub> = 50Ω, f = 100kHz, V <sub>COM</sub> = 1V <sub>RMS</sub> See Test Circuit Figure 5		-75		dB
Crosstalk	X <sub>TALK</sub>	C <sub>L</sub> = 5pF, R <sub>L</sub> = 50Ω, f = 100kHz, V <sub>COM</sub> = 1V <sub>RMS</sub> See Test Circuit Figure 6		-90		

3dB Bandwidth	$f_{3dB}$	See Test Circuit Figure 9	100	MHz
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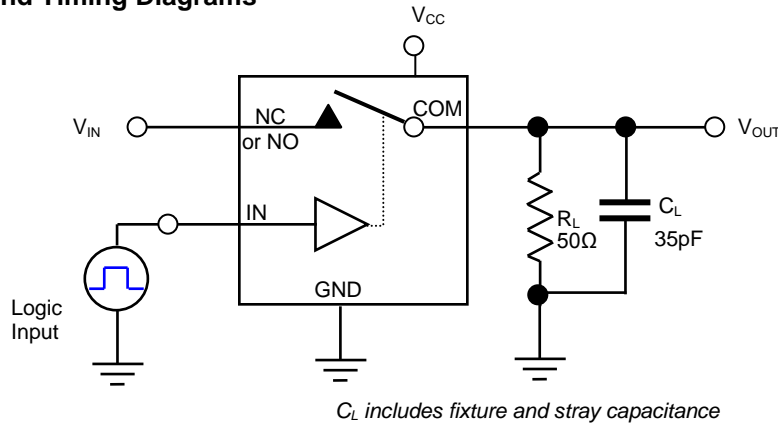
**Typical Characteristics**





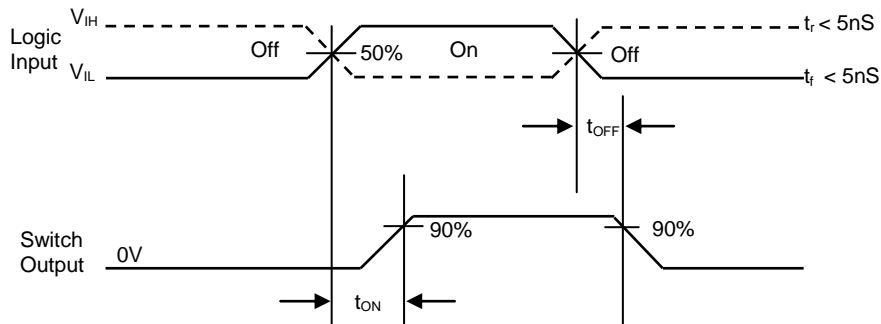
Note: Characteristics are guaranteed by design and are not production tested.

**Test Circuits and Timing Diagrams**



**Figure 1. AC Test Circuit**

**Note1.** Unused Input (NO or NC) must be grounded



*Logic Input Waveforms inverted for Switches that have opposite logic*

**Figure2 AC Waveforms**

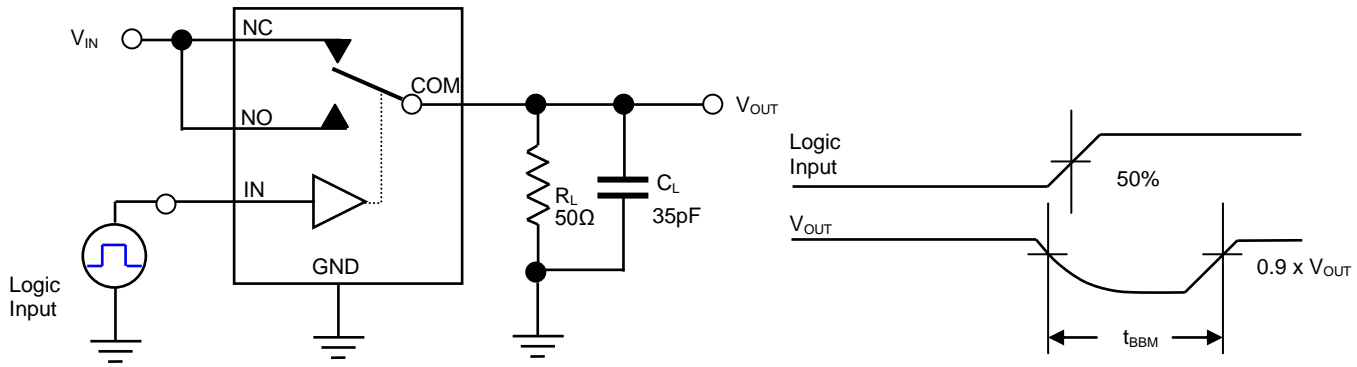


Figure 3. Break Before Make Interval Timing

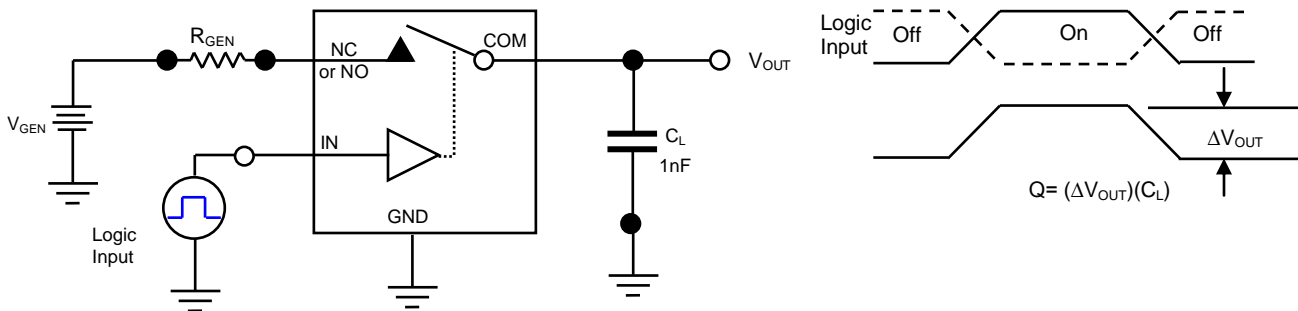
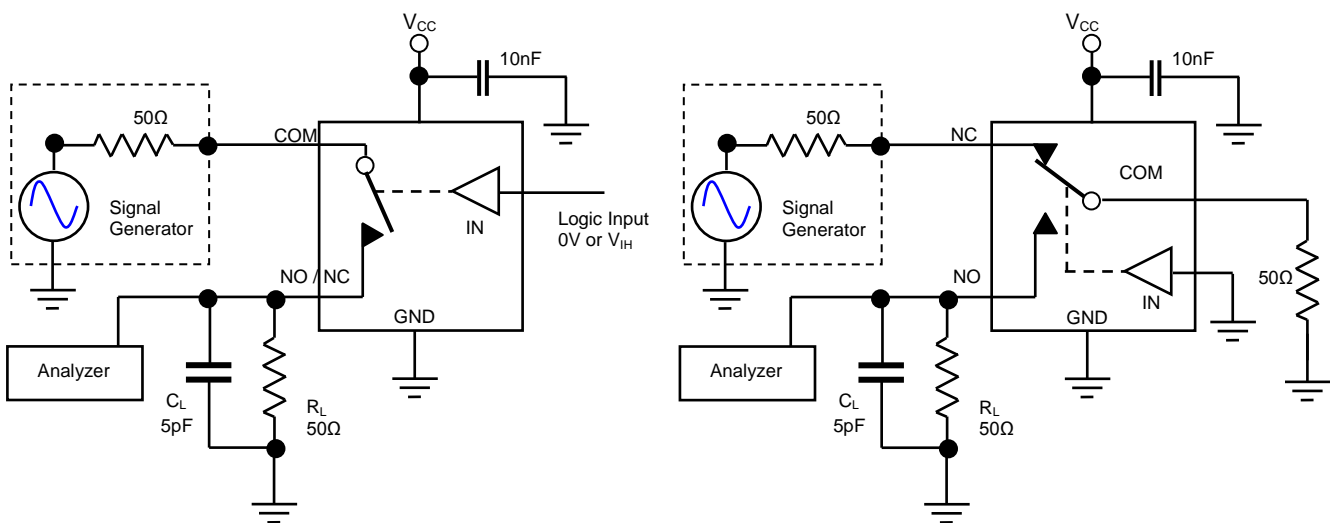
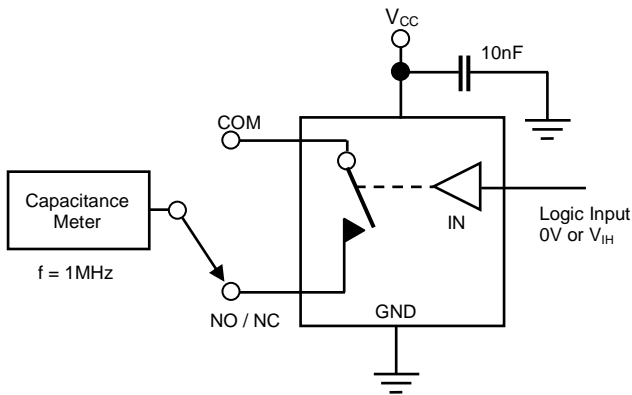


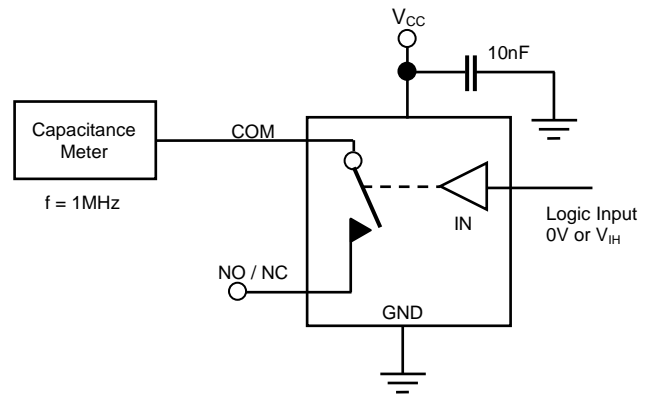
Figure 4. Charge Injection Test



**Figure 5. Off Isolation**

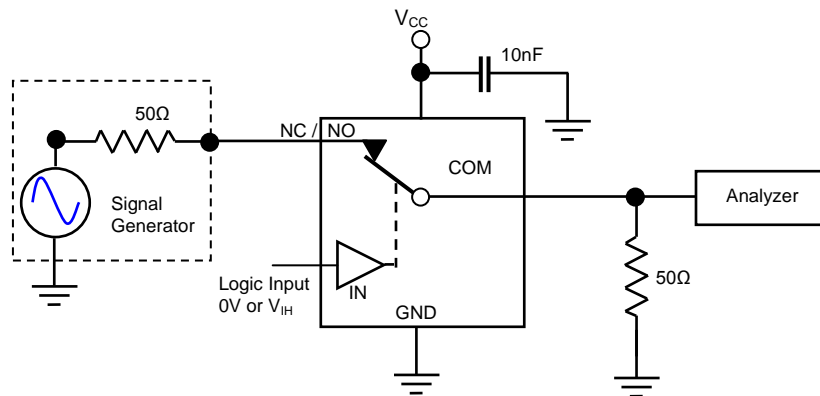


**Figure 6. Crosstalk**



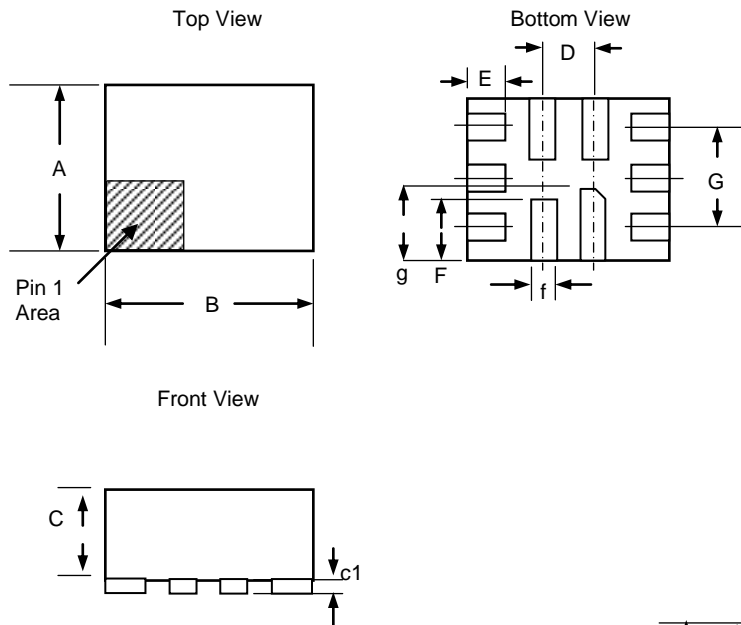
**Figure 7. Channel Off Capacitance**

**Figure 8. Channel On Capacitance**



**Figure 9. Bandwidth**

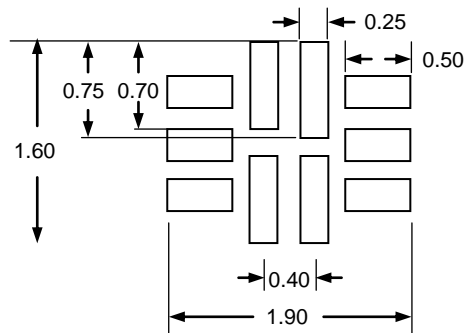
**Package Layout and Dimensions**



DIM	MIN	TYP	Max
A	1.25	1.30	1.35
B	1.55	1.60	1.65
C	0.50	0.55	0.60
D	0.40		
E	0.29	0.30	0.31
F	0.49	0.50	0.51
G	0.80 REF		
c	0.00 - 0.05		
c1	0.10 REF		
f	0.15	0.20	0.25
g	0.59	0.60	0.61

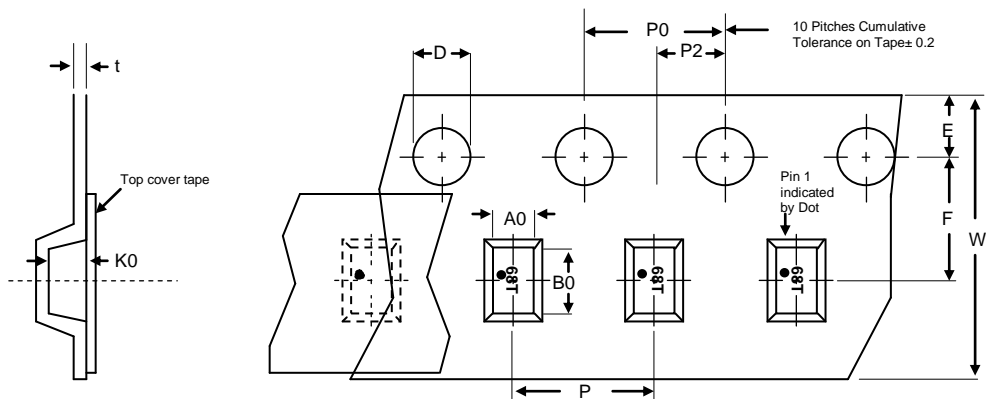
Note: Package Dimensions in millimeters

**Recommended Land Pattern**

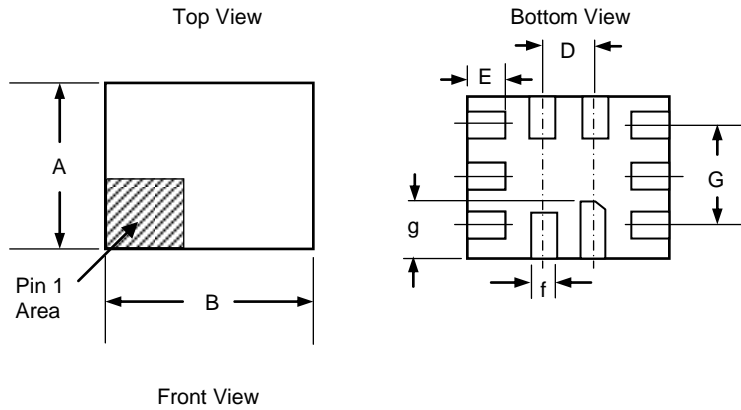


**Tape and Reel Specifications**

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	1.47±0.05	1.73±0.05	0.65±0.05	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25

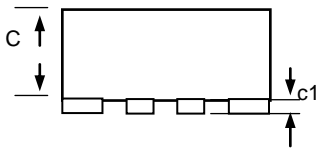


**Package Layout and Dimensions QFN-10**

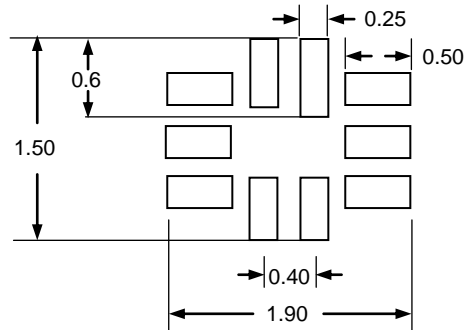


DIM	MIN	TYP	Max
A	1.35	1.40	1.45
B	1.75	1.80	1.85
C	0.50	0.55	0.60
D	0.40		
E	0.39	0.40	0.41
G	0.80 REF		
c1	0.10 REF		
f	0.15		
g	0.49	0.20	0.25

Note: Package Dimensions in millimeters

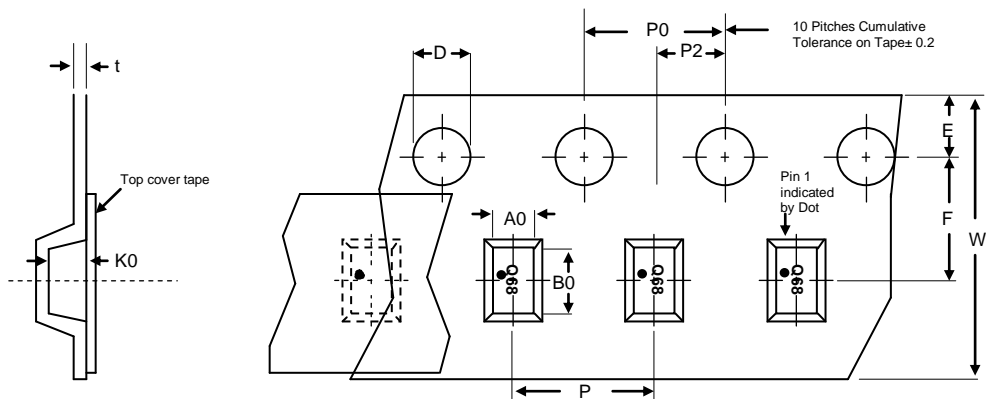


**Recommended Land Pattern**



**Tape and Reel Specifications**

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178 (7")	1.47±0.05	1.83±0.05	0.65±0.05	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25



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